09/21/2014

Discuss the structure of the Cache.

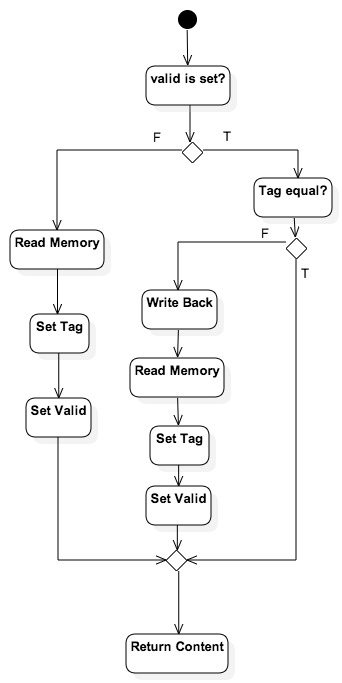
Direct-mapped.

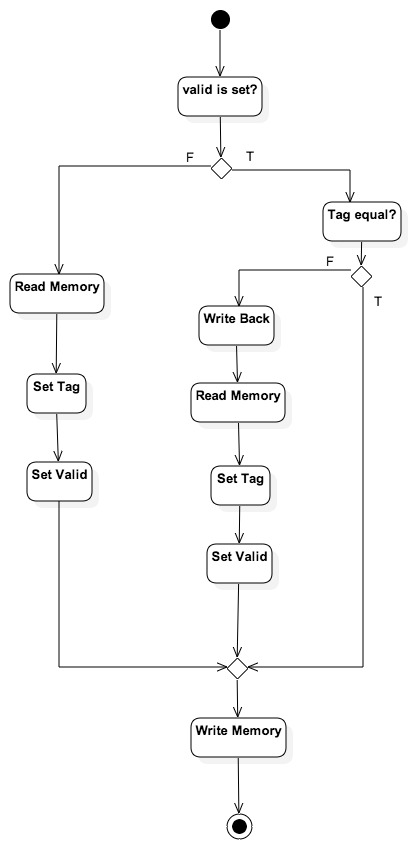
1 line per set

16 blocks per line

1 byte per block

The logical design of cache read and write:





09/28/2014

1. Test the cache.

2. Design the procedure of Program One

Five stage

Read in 20 numbers

Use IN to read in numbers

Use SOB to realize loop

Output 20 numbers

Use OUT to output numbers

Use SOB to realize loop

Read in one numbers

Use IN

Search the 20 numbers

Use SOB to realize loop

Keep the difference and the corresponding smallest number

Output the closest one

Use OUT

10/06/2014

Realize assembler.

Test the Program One

Discuss the UI

Coding, coding, coding…